REMARKS

Claims 1-12 and 26-37 stand rejected. Claims 1-7,have been rejected under 35 U.S.C. 102(b) as being anticipated by United States Patent No. 5,532,610 to Tsujide et al. Claims 8, 9, 21 and 22 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Tsujide in view of United States Patent No. 6,331,782 to White et al. Applicant respectfully submits that claims 1-25, as amended, are patentable and allowable over the cited art, as set forth in detail below.

Claim 1:

The has Examiner rejected claim 1 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,532,610 to Tsujide et al. Claim 1 reads as follows:

> 1. A wafer-interposer assembly comprising:
> a semiconductor wafer including a plurality of semiconductor die, each semiconductor die having a plurality of first electrical contact pads;
> an interposer **electrically connected and mechanically secured to the semiconductor wafer**, the interposer including a plurality of second electrical contact pads respectively **electrically connected and mechanically secured to at least some of the first electrical contact pads via soldered connections** such that the interposer and the semiconductor wafer are operable to be singulated into a plurality of chip assemblies, **each chip assembly comprising a semiconductor die and a portion of the interposer electrically connected and mechanically secured to one another via soldered connections**; and
> a communication interface integrally associated with the interposer and electrically connected to at least some of the second electrical contact pads. (Emphasis added)

In the Office Action, the Examiner explained his rejection of claims 1 and 26 as follows:

> With regard to claims 1 and 26, Tsujide et al show a semiconductor wafer to be tested 1 including a plurality of die where each die has a plurality of first contact pads, an interposer which is a wafer serving as a burn-in substrate 2 which includes a plurality of second contact pads which are respectively connected to at least some of the first contact pads by attachment elements 4, 5 such that the interposer and semiconductor wafer could be singulated into chip assemblies and a communication interface 9, 23 associated with the interposer and electrically connected to at least some of the second electrical contact pads.

[Office Action dated 4/6/05, p. 2]

As discussed in Applicant's prior response, Tsujide discloses a substrate for wafer level die burn-in that is designed to form a temporary mechanical and electrical connection with a wafer incorporating multiple devices under test. Figures 1 and 2 of the Tsujide reference appear as follows:

FIG. 1

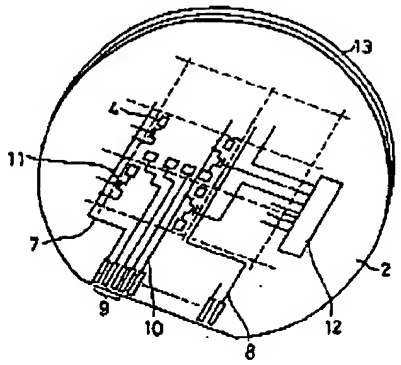
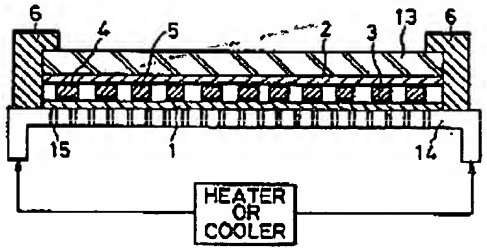


FIG. 2



In the prior response, Applicant argued that, contrary to the Examiner's assertion, Tsujide failed to disclose an apparatus in which the interposer and semiconductor wafer are "non-temporarily" connected to one another and "could be singulated into chip

assemblies." Upon viewing the above drawing figures of Tsujide and reading the associated written description, one of skill in the art would arrive at the inescapable conclusion that the "substrate 2" is only temporarily connected in an electrical manner to the "wafer 1". Further, to the extent that "substrate 2" of Tsujide could be considered to be mechanically connected to the "wafer 1", this relationship is also temporary.

There is nothing permanent or non-temporary about the contact between substrate 2 and wafer 1 of Tsujide. Each substrate 2 of Tsujide is designed to be re-used with each member of a set of individual wafers 1. They are not connected or secured to one another in a permanent manner, either electrically or mechanically. If an attempt were made to singulate the wafer 1 and substrate 2 of Tsujide into a plurality of chip assemblies, the result would be a plurality of wafer chips and a plurality of substrate chips, but the individual wafer chips and substrate chips would not be connected to one another and would therefore not be "chip assemblies" as that term is used within the context of the present application.

In response to Applicant's arguments on this point in the prior response, the Examiner responded as follows:

> Applicant argues that Tsujide et al does not non-temporarily electrically and mechanically connect the interposer to the semiconductor wafer. Nothing is permanent on Earth or the Heavens above and the apparatus of Tsujide et al is considered permanent if nobody takes it apart. Applicants do not define or give special meaning to "non-temporary" The

> term non-temporary does not even appear in Applicant's disclosure. "Non-temporary" could be argued to mean connected by solder but a solder joint can be considered as temporary in that a solder joint can be desoldered. The connection of interest in Tsujide et al is considered to be non-temporary.

[Office Action dated 4/6/05, pp. 2-3].

To whatever extent the Examiner's comment above may have been considered to apply to claims 1 and 26 prior to the present amendments, the Examiner's comment certainly could not be considered applicable to the claims as amended herein. Applicant has amended claims 1 and 26 to remove the qualifier "non-temporary" and to provide that the wafer and interposer are electrically connected and mechanically secured to one another via "soldered connections."

In light of the amendments herein, the distinctions between the teachings of Tsujide and the present claims are even more distinct. Whereas amended claim 1 recites an interposer "mechanically secured" to the semiconductor wafer, Tsujide fails to disclose mechanical securement between the wafer and the interposer. Whereas amended claim 1 recites a set of second electrical contact pads electrically connected and mechanically secured to at least some of the first electrical contact pads via "soldered connections," Tsujide discloses no such teaching, and in fact teaches the necessity that the wafer and interposer be **readily separable** from one another, thereby precluding any assertion that such a teaching is inherent to, or necessarily follows from,

Tsujide. Clearly, soldered connections between the wafer and interposer would not be at all workable in the context of Tsujide. Whereas amended claim 1 recites a wafer-interposer assembly operable to be singulated into a set of chip assemblies, with each chip assembly comprising a semiconductor die and a portion of the interposer **electrically connected and mechanically secured** to one another **via soldered connections**, Tsujide teaches no such limitation. Accordingly, Applicant respectfully submits that Tsujide fails to teach each and every limitation of amended claim 1, and therefore respectfully requests withdrawal of the outstanding §102(b) rejection of amended claim 1. Applicant further respectfully submits that Tsujide does not, alone or in combination with any other art, render claim 1 obvious. Accordingly, Applicant respectfully requests allowance of claim 1.

Claims 2-12

Claims 2-12 depend from claim 1 and add further limitations. Accordingly, each of claims 2-12 is allowable as being dependent on an allowable independent claim. Accordingly, Applicant respectfully requests withdrawal of the outstanding §102(b) and §103 rejections of claims 2-12.

Claim 26

As noted above, the Examiner rejected independent claim 26 on essentially the same rationale employed to reject independent claim 1. As amended, independent claim 26 reads as follows:

> 26. A wafer-interposer assembly comprising:
> a semiconductor wafer including a plurality of semiconductor die having a pattern of first electrical contact pads disposed thereon;
> an interposer **electrically connected and mechanically secured** to the semiconductor wafer, the interposer having a first surface with a pattern of second electrical contact pads disposed thereon, at least some of which correspond to and are **electrically connected and mechanically secured** to at least some of the first electrical contact pads **via soldered connections**, the interposer also having a second surface having a pattern of third electrical contact pads that are electrically connected to at least some of the second electrical contact pads, such that the interposer and the semiconductor wafer are operable to be singulated into a plurality of chip assemblies, each **including a semiconductor die and a portion of the interposer that remain electrically connected and mechanically secured to one another via soldered connections**; and
> a communication interface integrally associated with the interposer and electrically connected to at least some of the second electrical contact pads.

As noted above, Tsujide fails to teach or suggest that the substrate 2 and the wafer 1 of Tsujide are "mechanically secured" to one another via "soldered connections" or that the assembly is "operable to be singulated into a plurality of chip assemblies" as recited in independent claim 26. Further, claim 26 recites additional limitations not present in claim 1 which further distinguish this claim from Tsujide. Accordingly, Applicant respectfully requests withdrawal of the outstanding §102(b)

rejection of claim 26. Applicant further respectfully submits that Tsujide does not, alone or in combination with any other art, render claim 26 obvious. Accordingly, Applicant respectfully requests allowance of claim 26.

Claims 27-37

Claims 27-37 depend from claim 26 and add further limitations. Accordingly, each of claims 27-37 is allowable as being dependent on an allowable independent claim. Accordingly, Applicant respectfully requests withdrawal of the outstanding §102(b) and §103 rejections of claims 27-37.

Fee Statement

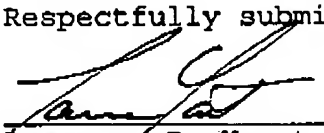
Applicant is submitting the present response in combination with a Request for Continued Examination and fee in the amount of $395.00. The number of independent claims has not been changed by way of the present Response. The total number of claims remains unchanged by way of the present Response. Applicant believes no additional fees are due with this Response. If additional fees are due or an overpayment has been made, please debit or credit our deposit account, Account No. 03-1130.

Conclusion

In view of the forgoing, the Examiner is respectfully requested to reconsider and withdraw the outstanding rejections to claims and allow claims 1-12 and 26-37 presented for consideration herein. Accordingly, a favorable action in the form of an early notice of allowance is respectfully requested. The Examiner is requested to call the undersigned for any reason that would advance the instant application to issue.

Dated this 17th day of June, 2005.

Respectfully submitted:



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